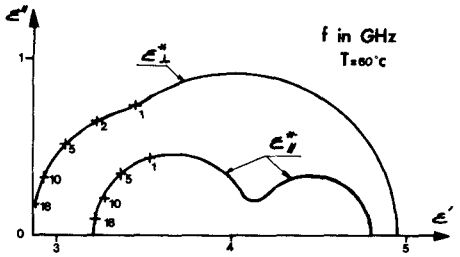

Fig. 4. Cole Cole plots of p-methoxyphenylazoxy-p'-butylbenzene in the nematic phase. $\epsilon_{\parallel}^*$: electric field $\parallel$ optical axis. $\epsilon_{\perp}^*$: electric field $\perp$ optical axis.

III. Calculation Procedure of the Sample Permittivity

Two stages are necessary in the calculation. First, a fictitious permittivity ϵ_f^* is calculated in the same way as before, assuming the cell to be coaxial of the same length and filled homogeneously with the sample. Then, the substance permittivity ϵ^* is deduced using a linear relationship

$$\epsilon_f^* = (1-\theta)\epsilon_q + \epsilon^*\theta$$
$$\epsilon^* = \epsilon' - j\epsilon'' \tag{10}$$

where ϵ_q is the quartz permittivity which is supposed to be real and θ is a filling factor. Then

$$\begin{cases} \epsilon' = \dfrac{\epsilon_f' - (1-\theta)\epsilon_q}{\theta} \\ \epsilon'' = \dfrac{\epsilon_f''}{\theta} \end{cases} \tag{11}$$

The filling factor θ can be calculated in the following way: in spite of the hybrid character of the cell, a quasi-TEM propagation-mode approximation can be assumed. Then, using a numerical method (finite difference method), it is easy to calculate ϵ_f' as a function of ϵ' by solving Laplace's equation in a cross-section plane of the cell [2].

We verified the linear relationship between ϵ_f' and ϵ'. The slope of the straight line gives θ.

The validity of all approximations is tested using standard liquids. Particularly, we have verified that no spurious higher order mode is propagating in the structure up to 18 GHz. In this bandwidth, the quasi-TEM approximation gave consistent results for low-loss dielectric materials with ϵ' values up to 7. In actual fact, the measurement accuracy is similar to the accuracy of usual measurement methods, namely the overall uncertainty is lower than 2 percent for ϵ' and 5 percent for ϵ''. Moreover, this method allows the direct plotting of spectra in the whole bandwidth.

IV. Applications

The process has been applied to the dielectric characterization of nematic liquid crystals in the microwave range. These substances are uniaxial, and the orientation of the sample optical axis with respect to the electric-field direction is achieved by using a magnetic field [3]. For example, we give in Fig. 4 the results obtained for a nematic compound in each direction of measurement: the parallel direction ($\epsilon_{\parallel}^*$), the perpendicular direction ($\epsilon_{\perp}^*$). The full line concerns the data we obtained by using conventional techniques [4]. The crosses are relative to the automatic process described before (only a few points are given). As we can see, the agreement is quite satisfying.

Such a process can be applied to other mesomorphic substances such as smectics, but also to liquids and isotropic or anisotropic solids. Obviously, in the last case, the sample optical axis has to be defined with respect to the electric field.

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Broad-band GaAs Monolithic Amplifier Using Negative Feedback

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Abstract—**A monolithic amplifier covering the 1–7-GHz frequency band has been fabricated using negative feedback. Small signal power gain of 6.0 dB ± 0.2 dB was achieved with maximum input and output VSWR of 2.3:1 and 1.7:1, respectively. Design considerations and processing techniques for active and passive elements are presented along with detailed performance data.**

I. Introduction

The use of distributed reactive matching elements and quadrature couplers in a balanced circuit are common in hybrid broad-band microwave amplifier designs. This technique has the advantages of simultaneous low reflection coefficients and maximum gain over bands up to several octaves. The higher dielectric constant of GaAs as compared to alumina results in only a 30 percent size reduction of distributed passive elements. For monolithic integrated circuits, where it is desirable to minimize the space used for passive elements, the use of lumped elements is an attractive alternative.

Negative feedback hybrid FET amplifiers are gaining popularity for broad-band application below 12 GHz. Several authors have presented data and design guidelines for selecting feedback elements to minimize input and output reflection coefficients consistent with maximum flat gain and minimum noise figure [1], [2]. Since these feedback designs employ lumped elements, this type of circuit is an obvious choice for monolithic applications.

The design of this monolithic amplifier utilizes experience gained in the development of various hybrid feedback designs nearing production. These hybrid circuits were used to obtain an insight into the FET geometry and circuit topology required to achieve desired amplifier performance.

II. Amplifier Design

The selection of a FET with sufficient transconductance is essential for the successful application of feedback techniques. Computer aided design and experience have shown that a 1000-μm gate width device with a transconductance of at least 80

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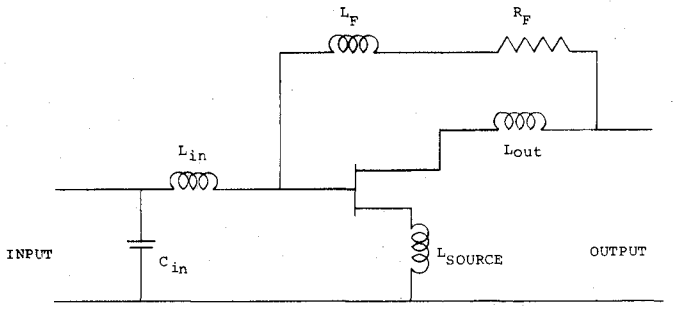


Fig. 1. Schematic diagram of negative feedback amplifier with low-pass input matching circuit.

mmho is adequate for feedback amplifiers in the 1–8-GHz range.

The device ultimately selected for this amplifier uses a four finger interdigital gate with drain-over-source air bridges. The device was processed with standard self aligned gate techniques resulting in a nominal gate length of 0.7 μm and dc electrical yields of about 50 percent[3]. GaAs active layers by both liquid phase epitaxy and direct ion implantation have been utilized. Nominal active layer doping and thickness are 2×10^{17} cm^{-3} and 0.3 μm, respectively. The final chip thickness is 0.125 ± 0.01 mm.

A schematic diagram of the desired topology is shown in Fig. 1. S-parameter data for the 1000-μm device are derived from device models and S-parameters measured on a similarly constructed 500-μm by 0.7-μm gate device used in production (Narda 5010 device). Passive elements R_f and L_f provide frequency-sensitive negative feedback, removing the 6 dB/octave gain slope inherent in the FET and pulling S_{11} into the center of the Smith Chart at the low end of the band. L_{in} and C_{in} form a low-pass filter completing the task of input impedance matching. The shunt capacitance to ground of C_{in} and the two adjacent bonding pads is calculated to be 0.032 pf, less than 7% of the design value for C_{in}, and is not included in the computer simulation. L_{out} is adjusted to optimize gain level, noise figure, and VSWR. The present design employs an interdigital capacitor, spiral inductors with air bridge center connections, and a thin-film metal resistor with several "taps" for adjustment of the feedback during assembly and testing.

III. Passive Element Realization

The accurate realization of passive elements, including capacitors, inductors, and resistors on the GaAs substrate is essential to the operation of the circuit. Furthermore, low-loss interconnections with short electrical lengths between elements are also important.

IV. Passive Element Calculation

To avoid the additional processing steps associated with dielectric overlay capacitors, an interdigital design was employed for this circuit. The formula used for the initial design is [4]

$$C_T = C(N-1)L$$

where

C_T = the total capacitance of the structure

N = number of lines

L = line length in millimeters

$$C = \epsilon_0(1+\epsilon r)\frac{K(k)}{K^1(k)}$$

where $K(k)$ and $K^1(k)$ are complete elliptic integrals and "k" is given by

$$k = \tan^2\left(\frac{\pi w}{4(w+s)}\right) \quad \text{and } k^1 = \sqrt{1-k^2}$$

where w is the line width and s is the spacing between lines.

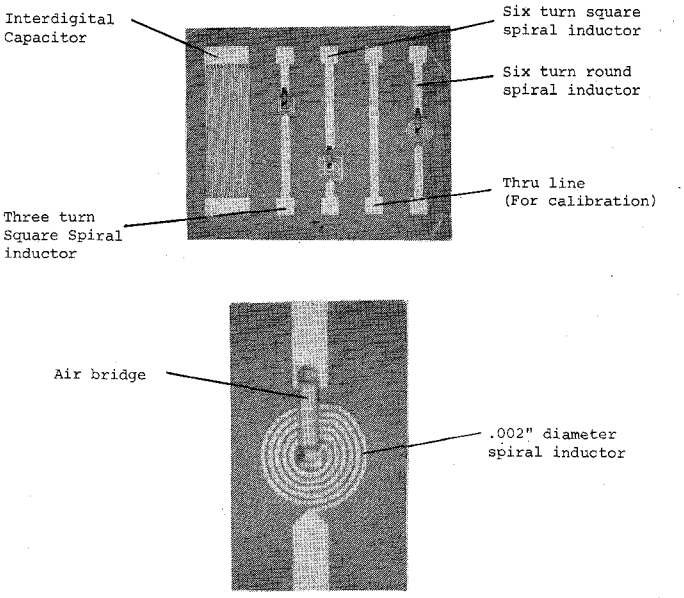


Fig. 2. Passive monolithic component test chip.

V. Spiral Inductors

The inductance of a spiral inductor can be calculated by [5]

$$L = \frac{0.8a^2n^2}{6a+10c}nH$$

where

n = the number of turns

$a = \frac{1}{2}(r_0 + r_i)$

$c = r_0 - r_i$

where r_i is the inside radius and r_0 is the outside radius.

VI. Passive Element Characterization

Since the values of most circuit elements in a monolithic amplifier cannot be modified after circuit fabrication, it is important to know the precise topology required to produce a given element value. It is also necessary to know the parasitics associated with each element so that these can be included in the amplifier design.

To obtain a good idea of these values, GaAs test chips were fabricated, each having several inductors and capacitors and a resistor. The element geometries were calculated, using the previous formulas, to result in values close to those required in the initial circuit design. These elements were arranged so that each one could be connected in series by wirebonding to 50 Ω input and output lines on alumina substrates. Also included on the test chip was a 50-Ω line for calibration purposes (Fig. 2).

The elements were then characterized on an automatic network analyzer using S-parameters. S-parameters have the advantage of being easily used by computerized circuit analysis programs. Using the results obtained by the measurements, a circuit model which included parasitics was obtained for each test element by adjusting the computed circuit model S-parameter data to match the measured data.

Fig. 3 shows the resulting circuit model for the interdigital

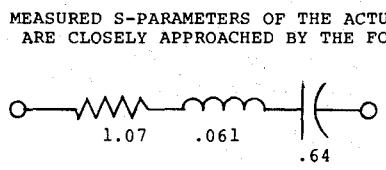
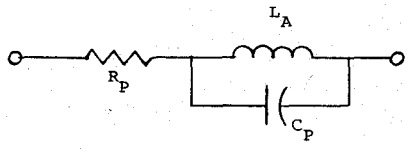


Fig. 3. Circuit model for interdigital capacitors.



# OF TURNS	CALCULATED INDUCTANCE L_c (nH)	PARASITIC RESISTANCE R_p (Ω)	PARASITIC CAPACITANCE C_p (pf)	ACTUAL INDUCTANCE L_A (nH)
2.3	.15	12.01	.045	.135
5.3	.93	35	.05	.88

Fig. 4. Circuit models for spiral inductors.

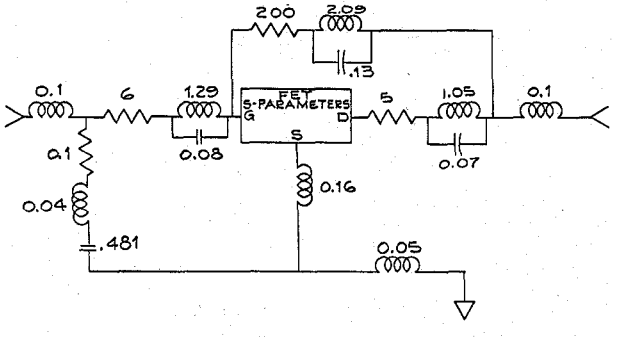


Fig. 5. Feedback amplifier equivalent circuit, including parasitic elements, after computer optimization.

capacitor; the discrepancy between calculated and modeled capacitance values is 11 percent.

Fig. 4 shows circuit-model measured and calculated values for two spiral inductors. The calculated value is 11-percent low for the small inductor and 6-percent low for the larger inductor. The high value of parasitic series resistance is due to the thin (3500 Å) gold metalization on the conductors.

VII. Final Amplifier Design

The feedback amplifier is fabricated on a GaAs substrate of identical thickness to that used for characterizing the passive elements. For this reason we assume that the parasitics included in these circuit models are sufficiently accurate and complete to be used in the final circuit design calculations. No other parasitics were included in the final design analysis.

The circuit model used for the final design computations is shown in Fig. 5. The values of the nonparasitic elements were optimized using standard CAD techniques. Since the intent of the program was to develop a practical amplifier capable of being cascaded with identical stages, a great deal of emphasis was placed on obtaining good VSWR's and flat gain across the 2–6-GHz band.

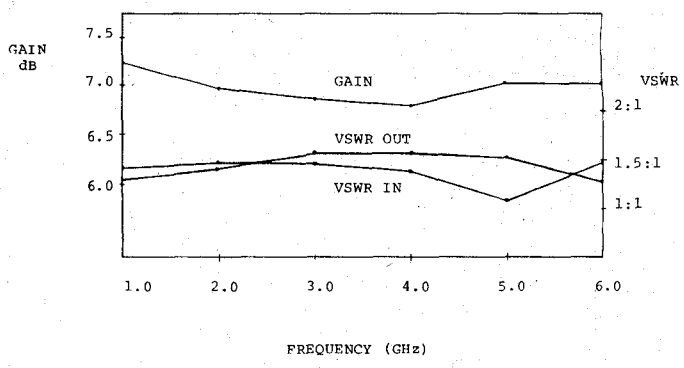


Fig. 6. Predicted gain and VSWR performance of the circuit in Fig. 5.

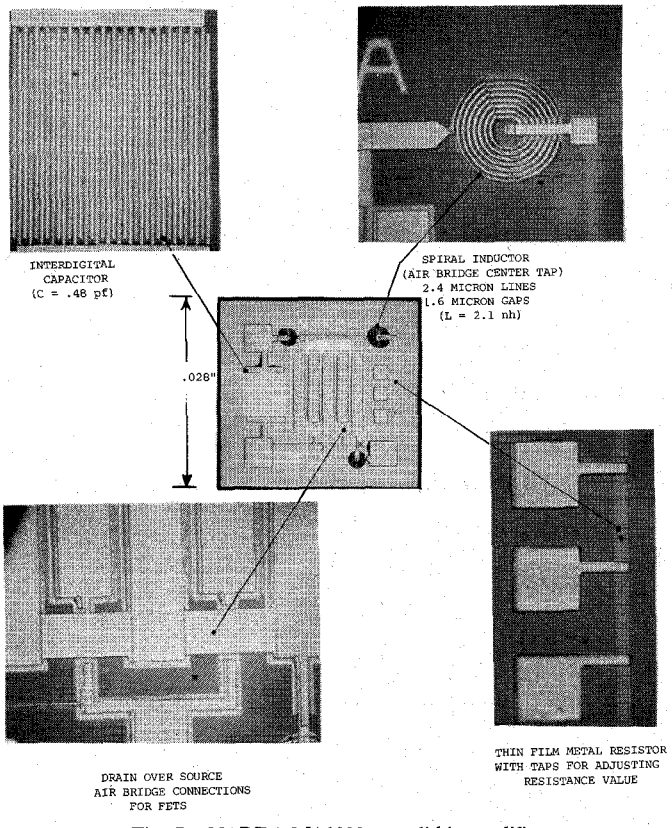


Fig. 7. NARDA MA1000 monolithic amplifier.

The predicted performance using the element values shown in Fig. 5 is given in Fig. 6.

VIII. Monolithic Amplifier Fabrication

The optimum value of feedback resistance predicted by computer simulation is 200 Ω. This resistor is fabricated using pure metal with 200 Å of excess thickness to compensate for an oxide film formed during postprocess stabilization baking.

In order to provide some tuning of the circuit during assembly and test, three "taps" are available for bypass wire bonds (see Fig. 7). The metal film resistor is designed such that a wire bond to the center tap results in a feedback resistance of 200 Ω.

The spiral inductors used for preliminary characterization were quite lossy as a result of thin metalization (3500 Å) to allow easy lift off of the pattern. In the final design, the resistive component was reduced somewhat by plating the coils with 20 000 Å of gold while simultaneously plating the air-bridge center connections.

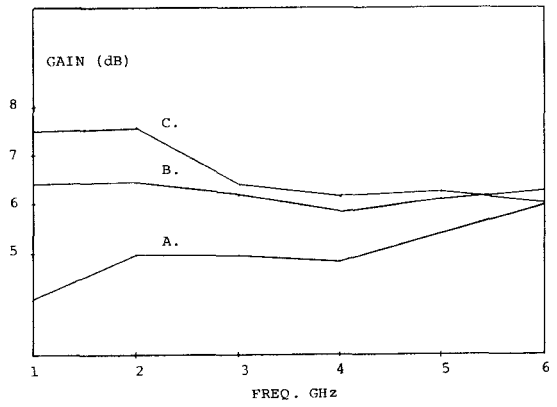


Fig. 8. Measured performance of chip S/N 001. Three curves are for different values of R_F. (A: $R_F = 241$; B: $R_F = 366\ \Omega$; C: $R_F = 491\ \Omega$.).

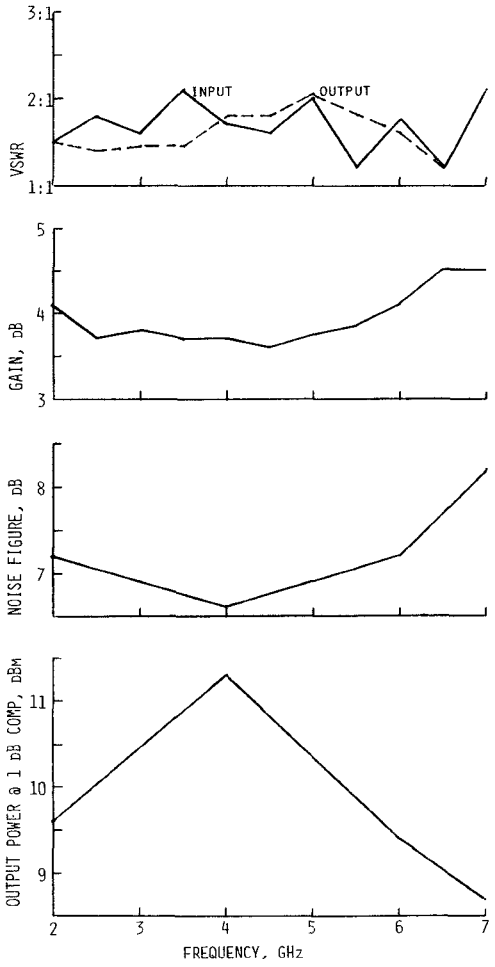


Fig. 9 Measured performance of S/N 002.

IX. Performance

The monolithic circuit was bonded into an alumina hybrid test fixture consisting of input and output 50-Ω microstrip lines with lumped-element bias networks. Gain performance from 1 to 6 GHz using various values of feedback resistance are shown in Fig. 8. As expected, the gain is improved with high values of feedback resistance at the expense of VSWR's and gain flatness. The optimum value of resistance (350 Ω) is substantially higher than expected and is presently being attributed to the excessive series resistance of the inductors. It is also believed that chip to chip variations and lower than predicted gain are the result of inconsistent gold plating in the inductors.

The noise figure and output power of a second amplifier chip was measured in the 2–7-GHz band and is shown in Fig. 9. We believe the noise figure can be reduced by another 2 dB by eliminating the losses in the input inductor.

X. Conclusion

The use of feedback techniques has been employed to realize monolithic amplifier chips in the 1–7-GHz band. Spiral inductors, interdigital capacitors, and thin film metal resistors were developed and integrated with self-aligned gate FET's to achieve 6-dB gain across this band.

Further work will center on the reduction of inductor loss and the integration of bias filter elements to improve gain and noise figure, and to reduce the size and cost of final amplifier assemblies.

Acknowledgment

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Slow Waves Guided by Parallel Plane Tape Guides

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***Abstract*—Waves guided by two parallel metallic plates of infinite extent, containing cuts at periodic intervals, are investigated for a number of cases with special emphasis upon the relative directions of the cuts in the top and bottom plates. Two fundamental slow-wave modes exist for all frequencies, in general. The latter are functions of tilt angles of the cuts, frequency, and plate separation. For tilt angles Ψ in the top and $\pm\Psi$ in the**

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